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# D480 PC-CARD USER'S GUIDE

**REVISION HISTORY**

| ISSUE | PAGES | AUTHOR | NOTES |
|---|---|---|---|
| A | 14 | PS | FIRST ISSUE |
| 1 | 22 | PS | MINOR CORRECTIONS+S/W SEC |
| 2 | 22 | PS | REMOVE INTERRUPT MENTION |
| 3 | 15 | BP | REMOVED SOFTWARE SECTION TO PCCARDGO.DOC |

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## 1.0 OVERVIEW

The D480 card is a general purpose Digital PIO card with the following features:

- 48 BI-DIRECTIONAL DIGITAL I/O LINES
- ANY I/O CAN BE PROGRAMMED AS AN INPUT OR AN OUTPUT
- ANY I/O CAN BE SET AS AN OPEN DRAIN TYPE DRIVER
- 47K PULL RESISTOR ON FIRST 40 I/Os TO A SWITCHABLE 0V OR 5V VOLTAGE SOURCE. POWER ON STATE IS PULL DOWN SO ALL I/Os DEFAULT TO LOW-HIZ. I/Os 41-48 HAVE 47K Vcc PULLUP.
- "SNAP-SHOT" MODE ALLOWS USER TO FREEZE INPUTS
- "SLEEP" MODE DISABLES CLOCK REDUCING POWER CONSUMPTION
- LOW POWER CONSUMPTION FOR PORTABLE APPLICATIONS
- TYPE II CARD IS PCMCIA 2.0 COMPLIANT
- FLEXIBLE CIRCUIT TERMINATES ALL I/O LINES IN A HIGH DENSITY IDC CONNECTOR OR TRIGGER TERMINAL BLOCKS FOR SIMPLE INTERFACING.

## 2.0 PROGRAMMING INTERFACE

The D480 decodes the incoming PCMCIA interface. It maps the CIS EPROM to 0-3FF,800-BFF etc. in attribute space. The range 400-7FF is occupied by the PCMCIA config register inside the FPGA (it repeats every byte). Both the CIS and config register are always active.

The config register is used as a master enable, as defined by PCMCIA 2.01. That is, when a valid config is written in bits0..5 the card's I/O interface may function. Until this has happened, the card's I/O interface is disabled. A config value of 1 will enable the card.

Bit6 of the register is don't care and bit7 of the register acts as a soft reset when set (the reset does not clear bit7 but a subsequent write to the config register to return bit 7 to zero should not attempt to load data into bits 6..0 of the register as they will still clear; this should be done as a separate operation.)

| | |
|---|---|
| BIT0 | Config value LSB |
| BIT1 | . |
| BIT2 | . |
| BIT3 | . |
| BIT4 | . |
| BIT5 | Config value MSB |
| BIT6 | Don't care |
| BIT7 | Apply internal RESET when set |

CONFIG Register at 400h in Attribute

All D480 functions are accessed via two I/O ports (as mapped by the host controller). The D480 only decodes A0, giving an Index register and a Data register (IR,DR). The IR is at the even address. It is 8-bits wide and is read/write. The IR selects which internal register is to be read/written via the DR (cf 82365 PCIC). The DR is also 8-bits wide. The D480 hence only uses nCE1 from the PCMCIA interface. It is the job of the host socket controller to map the IR and DR registers into the system's IO space.

The following list shows the indexes of the various registers in the D480 FPGA:

| IR | DR write | DR read | |
|---|---|---|---|
| 0 | IO1..8 DATA | I01..8 i/p STATE | BANK0 |
| 1 | IO9..16 DATA | I09..16 i/p STATE | BANK1 |
| 2 | IO17..24 DATA | I017..24 i/p STATE | BANK2 |
| 3 | IO25..32 DATA | I025..32 i/p STATE | BANK3 |
| 4 | IO33..40 DATA | I033..40 i/p STATE | BANK4 |
| 5 | IO41..48 DATA | IO BANK DIRECTIONS | |
| 6 | AUX SETUP REG | REVISION/MISC STATUS | |
| 7 | SETUP REG | SETUP REG | |
| 8 | BANK0 DIR CTRL | I041..48 i/p STATE | BANK5 |
| 9 | BANK1 DIR CTRL | NOT USED | |
| Ah | BANK2 DIR CTRL | NOT USED | |
| Bh | BANK3 DIR CTRL | NOT USED | |
| Ch | BANK4 DIR CTRL | NOT USED | |
| Dh | BANK5 DIR CTRL | NOT USED | |
| Eh | NOT USED | NOT USED | |
| Fh | NOT USED | NOT USED | |

## Index Allocations in the D480

The detailed operation of each register will now follow:

## *IOn..(n+7) DATA/STATE REGISTERS (IDX 0,1,2,3,4,5,8)*

If an IO pin is set as an output via the DIR CTRL register, then the DATA bit sent to that pin will directly control its output state. The 40 IO pins are grouped as 5 banks of 8 pins. All banks are identical EXCEPT bank 0 which has extra features. The byte sent to the DATA register for a bank corresponds bit-for-bit with the IO pins with the LSBit of the byte controlling the lowest numbered IO pin.

Reading the STATE register will return the bit-mapped state of the bank's IO pin input latches (transparent OR frozen depending on the mode of operation).

The power on state of all IO DATA registers is 00h.
***Note: Bank5 is written to via IDX 5 but it is read back via IDX8.***

## *IO BANK DIRECTIONS (IDX 5)*

This is an 8-bit read only register. With all but the exception of BANK0, a BANK's set of 8 IO pins can only be set up as all inputs or all outputs. BANK0 has finer resolution to allow any number of inputs and outputs within the 40 total IO pins. The structure of the register is as follows:

| | |
|---|---|
| BIT0 | DIRECTION OF BANK0 PIN1 |
| BIT1 | DIRECTION OF BANK1 |
| BIT2 | DIRECTION OF BANK2 |
| BIT3 | DIRECTION OF BANK3 |
| BIT4 | DIRECTION OF BANK4 |
| BIT5 | DIRECTION OF BANK0 PIN2 |
| BIT6 | DIRECTION OF BANK0 PINS3&4 |
| BIT7 | DIRECTION OF BANK0 PINS5,6,7&8. |

A '1' in any bit position means that the IO pin is an output.
***Note: Bank5 direction is read back on Bit6 of IDX 6.***

## *AUX SETUP REGISTER (IDX 6)*

This register is write only and provides a "grab-bag" of left over control bits. Its layout is as follows:

| | |
|---|---|
| BIT0 | IOPULLUP DIRECTION 0=pull down 1=pull up (POS=0) (first 40 IO pins have 47K connected to a buffered version of this signal). |
| BIT1 | NOT USED |
| BIT2 | NOT USED |
| BIT3 | NOT USED |
| BIT4 | MUST BE '0' (POS=0) |
| BIT5..7 | RESERVED (KEEP AT '0') |

NB: POS="POWER ON STATE" (and after a reset)

## *REVISION/MISC STATUS REGISTER (IDX 6)*

The bottom 6 bits give the chip ID and revision code. The top two bits are used for status monitoring, as follows:

| | |
|---|---|
| BIT0 | ID CODE LSBit |
| BIT1 | . |
| BIT2 | ID CODE MSBit |
| BIT3 | REV CODE LSBit |
| BIT4 | . |
| BIT5 | REV CODE MSBit |
| BIT6 | BANK 5 DIRECTION |
| BIT7 | 0 |

The ID code will be 5 (for D480). The REV code will follow the revision of the GATE ARRAY and is currently at 1.

## *SETUP REGISTER (IDX 7)*

This register controls the major housekeeping functions of the FPGA. Its layout is as follows (NB POS="Power On State"):

BIT0 NOT USED
BIT1 NOT USED
BIT2 NOT USED
BIT3 NOT USED
BIT4 LATCHMODEEN POS=0. When BIT 4 is high, the state of data present on BANK inputs is frozen in transparent latches. This is "snapshot". When BIT4 is low, the latches operate in transparent mode.
BIT5 NOT USED
BIT6 NOT USED
BIT7 NOT USED

## *BANKn DIR CTRL REGISTERS (IDX 8,9,A,B,C,D)*

These six registers control whether each bank is set for input/output/open drain operation. BANK0 differs from the other 5 banks. The register layout is as follows:

BANK0 DIR CTRL (IDX 8)

| | |
|---|---|
| BIT0 | IOPIN 1 DIRECTION |
| BIT1 | IOPIN 2 DIRECTION |
| BIT2 | IOPINS 3&4 DIRECTION |
| BIT3 | IOPINS 5,6,7&8 DIRECTION |
| BIT4 | SET BANK OUTPUTS TO OPEN DRAIN OPERATION |
| BIT5..7 | NOT USED |

BANK1,2,3,4&5 DIR CTRL (IDX 9..D respectively)

| | |
|---|---|
| BIT0 | BANK DIRECTION |
| BIT1 | NOT USED |
| BIT2 | NOT USED |
| BIT3 | NOT USED |
| BIT4 | SET BANK OUTPUTS TO OPEN DRAIN OPERATION |
| BIT5..7 | NOT USED |

In all cases, a logic '1' sets the IOPIN(s) or BANK to an output. A logic '1' in BIT 4 enables the open drain function. In this mode, each IOPIN from 1 to 40 is pulled via a 47K resistor to Vpull as set via the AUX SETUP REGISTER. The IOPIN rise time in this mode is load dependant. The IOPIN will typically reach between 4.6v and 4.8v when pulled high although the exact level will depend on the host-controllers VCC level.
By programming an IOPIN as an input, Vpull and the IOPIN's 47K resistor could be used for diagnostics e.g. trying to pull a signal line around to test that it is not being driven.
***Note: Bank 5 I/Os each have a permanent Vcc 47K pull up.***

# 3.0 HARDWARE SPECIFICATION

**DIGITAL I/O:**

- Programmable as Input/Output allowing any number of inputs and outputs from 0 to 48.

- An I/O set as an output can be read-back for verification purposes. An I/O set as an output can also be set into open drain mode. Input levels are TTL compatible.

- Output drivers are CMOS, with typically 4mA source/sink at TTL levels.

- All I/Os from 1 to 40 have a 47K pull up/down resistor and will all power up as inputs. The pull direction is programmable to 0v or 5v (globally), defaulting to 0v on power-up.

- Readback can be "asynchronous" or latched. Asynchronous mode relies on software polling, whereas latched mode uses a control bit to strobe the input data into internal holding latches. This applies globally to all I/Os set as inputs.

- All reads/writes to the card are 8-bits wide. All data and configuration registers can be read as well as written to make "bit-wise" updates easy.

**MISCELLANEOUS**

- PCMCIA interface uses 2-I/O ports to communicate with the card (Index & Data registers). These can be located on any even system I/O address. All transactions are 8-bits wide.

- Card has a fully PCMCIA compliant Card Information Structure.

- Type II card uses a pair of highly durable 30-way flexible circuits and a connector PCB to interface all user signals. Two options are available: 60 way trigger terminal interface or 60 way half pitch IDC interface. Both options are interchangeable.

- Power consumption is typically 3mA at 5V with no loads

- "Hot-insertion" will not generate any spurious outputs on the first 40 digital I/O lines.

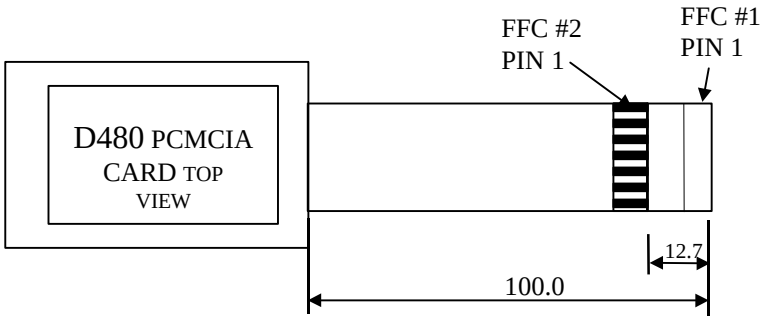
## PINOUTS

Signals are carried off the D480 using two 30 way Flat Flexible Conductors (FFC's). These are 1mm pitch types with ends prepared to fit into HIROSE FH10A-30S-1SHB type SMT connectors. The pitch between these should be 12.7mm with one mounted on the top surface and one of the rear surface of the connecting PCB. Care should be taken that the pin numbers on these connectors is made to match the pin numbering on the FFCs as shown below.

| FFC#2 PIN NUMBER | SIGNAL | FFC#1 PIN NUMBER | SIGNAL |
|---|---|---|---|
| 1 | GND | 1 | GND |
| 2 | IOPIN2 | 2 | IOPIN1 |
| 3 | IOPIN4 | 3 | IOPIN3 |
| 4 | IOPIN6 | 4 | IOPIN5 |
| 5 | IOPIN8 | 5 | IOPIN7 |
| 6 | IOPIN10 | 6 | IOPIN9 |
| 7 | IOPIN12 | 7 | IOPIN11 |
| 8 | IOPIN14 | 8 | IOPIN13 |
| 9 | IOPIN16 | 9 | IOPIN15 |
| 10 | IOPIN18 | 10 | IOPIN17 |
| 11 | IOPIN20 | 11 | IOPIN19 |
| 12 | IOPIN22 | 12 | IOPIN21 |
| 13 | IOPIN24 | 13 | IOPIN23 |
| 14 | IOPIN45 | 14 | IOPIN41 |
| 15 | IOPIN45 | 15 | IOPIN42 |
| 16 | IOPIN46 | 16 | IOPIN43 |
| 17 | N/C | 17 | N/C |
| 18 | IOPIN47 | 18 | VCC (200mA MAX) |
| 19 | IOPIN48 | 19 | GND |
| 20 | GND | 20 | IOPIN44 |
| 21 | GND | 21 | IOPIN46 |
| 22 | GND | 22 | GND |
| 23 | IOPIN25 | 23 | IOPIN26 |
| 24 | IOPIN27 | 24 | IOPIN28 |
| 25 | IOPIN29 | 25 | IOPIN30 |
| 26 | IOPIN31 | 26 | IOPIN32 |
| 27 | IOPIN33 | 27 | IOPIN34 |
| 28 | IOPIN35 | 28 | IOPIN36 |
| 29 | IOPIN37 | 29 | IOPIN38 |
| 30 | IOPIN39 | 30 | IOPIN40 |

### D480 PINOUTS

**NB: FFC#2 CONDUCTORS FACE UP, FFC#1 CONDUCTORS FACE DOWN**



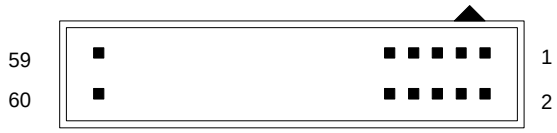
## IDC BREAKOUT BOARD OPTION:

60 WAY HALF PITCH CONNECTOR TYPE: HIROSE HIF6H-60PA-1.27DS (PLUG) MATES WITH HIROSE HIF6H-60D-1.27R (CABLE MOUNTED SOCKET).

PINOUT:

| PIN NUMBER | SIGNAL |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | IOPIN2 |
| 4 | IOPIN1 |
| 5 | IOPIN4 |
| 6 | IOPIN3 |
| 7 | IOPIN6 |
| 8 | IOPIN5 |
| 9 | IOPIN8 |
| 10 | IOPIN7 |
| 11 | IOPIN10 |
| 12 | IOPIN9 |
| 13 | IOPIN12 |
| 14 | IOPIN11 |
| 15 | IOPIN14 |
| 16 | IOPIN13 |
| 17 | IOPIN16 |
| 18 | IOPIN15 |
| 19 | IOPIN18 |
| 20 | IOPIN17 |
| 21 | IOPIN20 |
| 22 | IOPIN19 |
| 23 | IOPIN22 |
| 24 | IOPIN21 |
| 25 | IOPIN24 |
| 26 | IOPIN23 |
| 27 | IOPIN45 |
| 28 | IOPIN41 |
| 29 | IOPIN45 |
| 30 | IOPIN42 |
| 31 | IOPIN46 |
| 32 | IOPIN43 |
| 33 | N/C |
| 34 | N/C |
| 35 | IOPIN47 |
| 36 | Vcc (200mA MAX) |
| 37 | IOPIN48 |
| 38 | GND |
| 39 | GND |
| 40 | IOPIN44 |
| 41 | GND |
| 42 | IOPIN46 |
| 43 | GND |
| 44 | GND |
| 45 | IOPIN25 |
| 46 | IOPIN26 |
| 47 | IOPIN27 |
| 48 | IOPIN28 |
| 49 | IOPIN29 |
| 50 | IOPIN30 |
| 51 | IOPIN31 |
| 52 | IOPIN32 |
| 53 | IOPIN33 |
| 54 | IOPIN34 |

| | |
|---|---|
| 55 | IOPIN35 |
| 56 | IOPIN36 |
| 57 | IOPIN37 |
| 58 | IOPIN38 |
| 59 | IOPIN39 |
| 60 | IOPIN40 |




VIEW ON PINS

# 4. SOFTWARE

## *4.1 UNIVERSAL DRIVER*

The PCCARDGO “universal driver” is used to act as a surrogate Card Services client for an end user application. This device driver simplifies greatly the enumeration process and configuration management task for your application.

The driver is supplied on the diskette provided.

Please refer to PCCARDGO.DOC for further information.

## *4.2 C SOURCE CODE*

On the diskette provided are several .C and .H files that provide a convenient starting point for you to create your own application. The files are located in a directory with the same name as this card.

## 5.0 OPERATIONAL PRECAUTIONS

Unless otherwise stated, all voltage levels are referenced to the **D480**'s "GND" pins.

- DON'T LEAVE ACTIVE SIGNALS CONNECTED TO THE DIGITAL IOPINs OR OTHER DIGITAL LINES THAT ARE CAPABLE OF SOURCING MORE THAN A FEW mA WHILST THE D480 ITSELF IS UNPOWERED. THIS COULD LEAD TO "REVERSE POWERING" THE CARD VIA ITS INPUTS WHICH CAN CAUSE LATCH-UP AND DESTRUCTION OF INTERNAL CMOS DEVICES. IF THERE IS A POSSIBILITY OF THIS CONDITION OCCURRING, YOU ARE ADVISED TO CONNECT SERIES RESISTORS BETWEEN YOUR DRIVERS AND THE D480'S SIGNALS TO AFFECT CURRENT LIMITING (TYP 4K7). REMEMBER THAT THIS WILL SLOW THE EDGES OF THE DIGITAL SIGNALS.
- DON'T DRAW EXCESSIVE CURRENT FROM VCC. THE LIMITS ARE SHOWN IN THE PINOUT TABLE. DOING SO WILL ADVERSELY EFFECT THE D480'S PERFORMANCE AND COULD CAUSE DAMAGE.
- DON'T APPLY DIGITAL INPUTS TO THE D480 THAT ARE GREATER THAN (System Vcc + 0.5v) WHERE "System Vcc" IS THE LEVEL PROVIDED ON THE D480'S VCC OUTPUT PIN. DOING SO WILL DAMAGE THE D480. LIKEWISE, DON'T APPLY LEVELS THAT ARE LESS THAN -0.5v TO THE DIGITAL INPUTS.
- DON'T SHORT CIRCUIT ANY OF THE D480'S OUTPUTS TO GROUND OR TO OTHER OUTPUTS. THIS WILL DAMAGE THE D480.